STRUCTURE Silicon Monolithic Integrated Circuit
TYPE Step down 2ch DC/DC converter Controller for Lap top PC
PRODUCT SERIES **BD9535MUV**
FEATURES
- Built in 2ch H^{3}REG DC/DC controller
- Switching Frequency Variable (f=200kHz～600kHz)
- Built in PGOOD function

OABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage 1	V_{CC}	7 *1	V
Input Voltage 2	V_{DD}	7 *1	V
Input Voltage 3	V_{IN}	30 *1	V
BOOT Voltage	$V_{BOOT1/2}$	35 *1	V
BOOT-SW Voltage	V_{BOOT1}-V_{SW1}, V_{BOOT2}-V_{SW2}	7 *1	V
HG-SW Voltage	V_{HG1}-V_{SW1}, V_{HG2}-V_{SW2}	7 *1	V
LG Voltage	$V_{LG1/2}$	V_{DD}	V
Output Voltage Setting Voltage	$V_{REF1/2}$	V_{CC}	V
Output Voltage	$V_{IS+1/2}$, $V_{IS-1/2}$	V_{CC}	V
SS Voltage	$V_{SS1/2}$	V_{CC}	V
FS Voltage	V_{FS}	V_{CC}	V
VREG Voltage	V_{REG}	V_{CC}	V
Current Limit Setting Voltage	$V_{ILIM1/2}$	V_{CC}	V
Logic Input Voltage	$V_{EN1/2}$	7 *1	V
PGOOD Voltage	$V_{PGOOD1/2}$	7 *1	V
CE Voltage	$V_{CE1/2}$	V_{REG}	V
Power Dissipation 1	Pd1	0.38*2	W
Power Dissipation 2	Pd2	0.88*3	W
Power Dissipation 3	Pd3	2.06*4	W
Power Dissipation 4	Pd4	4.56*5	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd, ASO, and Tjmax=150℃.
*2 Reduced by 3.0mW for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*3 Reduced by 7.0mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 0mm^2))
*4 Reduced by 16.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm^2, 2nd and 3rd copper foil area : 5505mm^2))
*5 Reduced by 36.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5505mm^2))

OOPERATING CONDITIONS (Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	V_{CC}	4.5	5.5	V
Input Voltage 2	V_{DD}	4.5	5.5	V
Input Voltage 3	V_{IN}	3.0	28	V
BOOT Voltage	$V_{BOOT1/2}$	4.5	33	V
SW Voltage	$V_{SW1/2}$	-0.7	28	V
BOOT-SW Voltage	V_{HG1}-V_{SW1}, V_{HG2}-V_{SW2}	4.5	5.5	V
Logic Input Voltage	$V_{EN1/2}$	0	5.5	V
Output setting voltage	$V_{REF1/2}$	0.7	2.0	V
Is Input Voltage	$V_{IS+1/2}$, $V_{IS-1/2}$	0.7	2.0	V
Minimum ON Time	tonmin	-	100	nsec

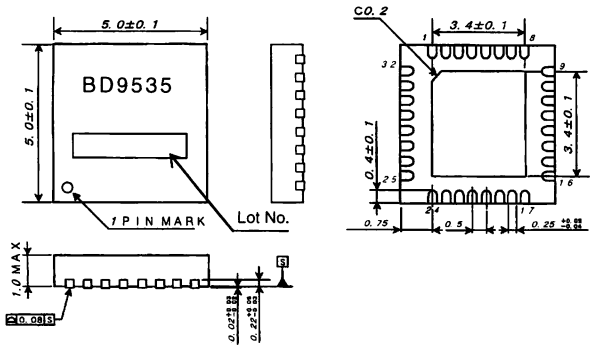
★ This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25℃ V_{CC}=5V,V_{DD}=5V,$V_{EN1/2}$=3V,V_{IN}=12V,$V_{REF1/2}$=1.8V,R_{FS}=68kΩ)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
[Whole Device block]						
VCC Bias Current	Icc	-	1.4	2.0	mA	
VIN Bias Current	IIN	-	200	400	μA	
VCC Standby Current	Istb	-	0	20	μA	VEN1=VEN2=0V
VIN Standby Current	IIN_stb	-	0	40	μA	VEN1=VEN2=0V
EN Low Voltage1,2	VEN_low1,2	GND	-	0.8	V	
EN High Voltage1,2 (Forced continuous mode)	VENth_con1,2	2.3	-	3.8	V	
EN High Voltage1,2(SLLM™)	VENth_sllm1,2	4.2	-	5.5	V	
EN Bias Current1,2	IEN1,2	-	7	10	μA	
VREG Voltage	VREG	2.480	2.500	2.520	V	IREG=500μA Ta=-10～100℃
[Under Voltage Locked Out block]						
VCC threshold voltage	Vcc_UVLO	4.1	4.3	4.5	V	VCC:Sweep up
VCC hysteresis voltage	dVcc_UVLO	100	160	220	mV	VCC:Sweep down
VIN threshold voltage	VIN_UVLO	2.4	2.6	2.8	V	VIN:Sweep up
VIN hysteresis voltage	dVIN_UVLO	100	160	220	mV	VIN:Sweep down
VREG threshold voltage	VREG_UVLO	2.0	2.2	2.4	V	VREG:Sweep up
VREG hysteresis voltage	dVREG_UVLO	100	160	220	mV	VREG:Sweep down
[Over Voltage Protection block]						
VOUT Threshold Voltage 1,2	VOUT_OVP1,2	VREF×1.15	VREF×1.20	VREF×1.25	V	
[Power Good block]						
VOUT POWER GOOD LOW Voltage1,2	VPGOOD_low1,2	VREF×0.87	VREF×0.90	VREF×0.93	V	
VOUT POWER GOOD HIGH Voltage1,2	VPGOOD_high1,2	VREF×1.07	VREF×1.10	VREF×1.13	V	
Discharge ON Resistance1,2	Ron_PGOOD1,2	-	1.0	2.0	kΩ	
Delay Time1,2	tPGOOD1,2	150	250	350	μsec	
[H³REG™ block]						
ON Time1	ton1	400	500	600	nsec	RFS=68kΩ
MAX ON Time1	tonmax1	1.8	3.0	4.2	μsec	
MIN OFF Time1	toffmin1	500	600	700	nsec	
ON Time2	ton2	250	350	450	nsec	RFS=68kΩ
MAX ONTime2	tonmax2	1.0	2.1	3.2	μsec	
MIN OFF Time2	toffmin2	500	600	700	nsec	
[FET Driver block]						
HG upper side ON Resistance1,2	RHGhon1,2	-	3.0	6.0	Ω	
HG Lower side ON Resistance 1,2	RHGlon1,2	-	2.0	4.0	Ω	
LG upper side ON Resistance 1,2	RLGhon1,2	-	2.0	4.0	Ω	
LG Lower side ON Resistance 1,2	RLGlon1,2	-	0.5	1.0	Ω	
[Soft start block]						
Charge Current 1,2	Iss1,2	1.4	2	2.6	μA	
Discharge Current 1,2	Iss_dis1,2	1.4	2	2.6	μA	
Discharge Threshold Voltage 1,2	Vss_disth1,2	-	0.1	0.2	V	
Standby Voltage 1,2	Vss_STB1,2	-	-	50	mV	
[Current Limit block]						
Current Limit Threshold Voltage1_1,2	Vilim11,2	40	50	60	mV	VILIM1,2=0.5V
Current Limit Threshold Voltage2_1,2	Vilim21,2	170	200	230	mV	VILIM1,2=2.0V
[Output Voltage Sense block]						
Vis offset voltage1,2	VIS_off1,2	1.790	1.800	1.810	V	Ta=-10～100℃
REF bias current1,2	IREF1,2	-150	0	150	nA	
Is+ input current1,2	Iis+1,2	-1.0	0	1.0	μA	Vis+1,2=1.8V
Is- input current1,2	Iis-1,2	-1.0	0	1.0	μA	Vis-1,2=1.8V
[SCP block]						
Threshold Voltage1,2	Vthscp1,2	VREF×0.65	VREF×0.7	VREF×0.75	V	
Delay Time 1,2	tscp1,2	0.5	1	1.5	msec	

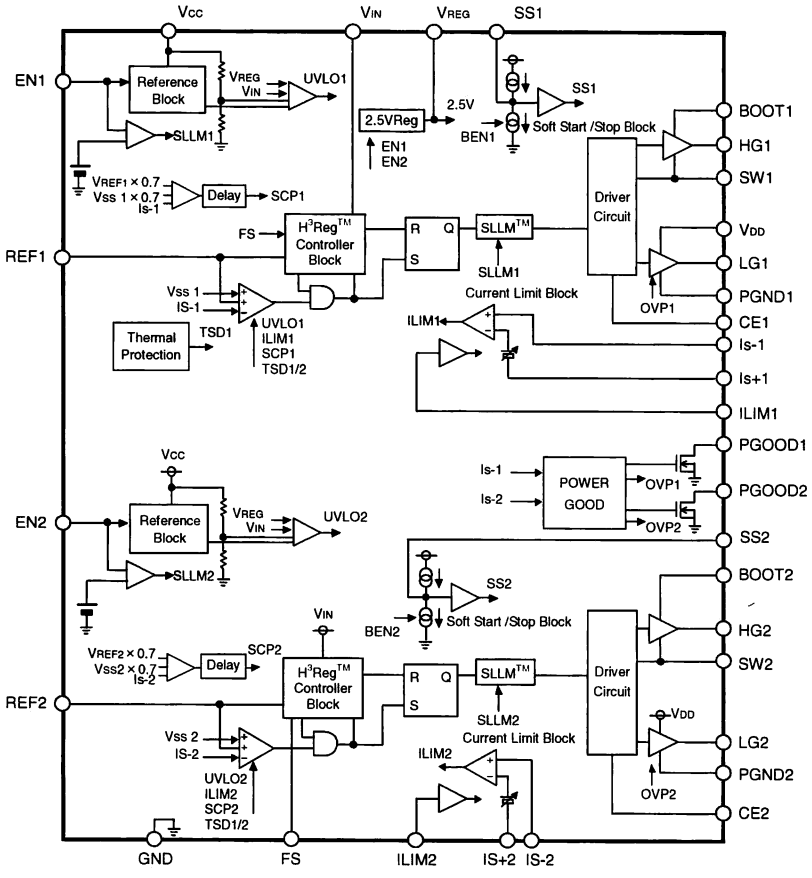
OPHYSICAL DIMENSIONS



(UNIT:mm)

VQFN032-V5050

OBLOCK DIAGRAM

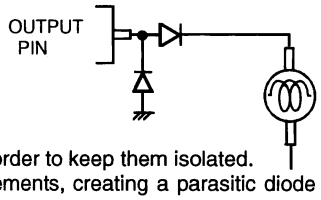


OPIN No., PIN Name

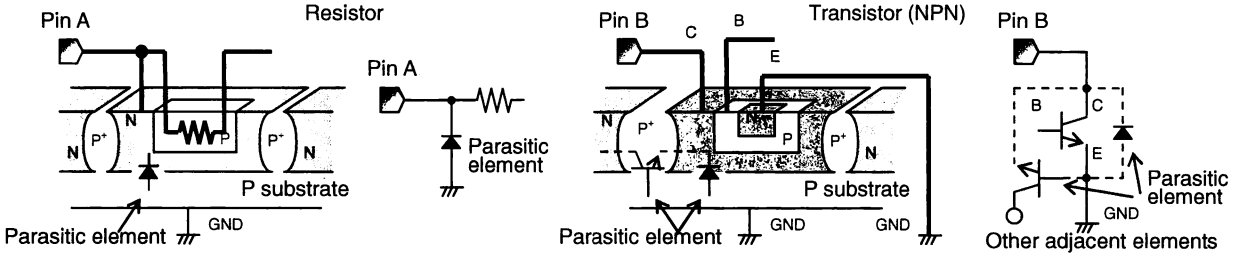
PIN No.	PIN name
1	BOOT1
2	CE1
3	PGOOD1
4	EN1
5	SS1
6	ILIM1
7	REF1
8	VREG
9	FS
10	Is-1
11	Is+1
12	GND
13	Vcc
14	Is+2
15	Is-2
16	VIN
17	REF2
18	ILIM2
19	SS2
20	EN2
21	PGOOD2
22	CE2
23	BOOT2
24	HG2
25	SW2
26	PGND2
27	LG2
28	VDD
29	LG1
30	PGND1
31	SW1
32	HG1
Bottom	FIN

ONOTES FOR USE

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. GND voltage
   The potential of GND, PGND1, PGND2 pin must be minimum potential in all operating conditions.
3. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
4. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
5. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
6. ASO
   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.
7. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.
8. Electrical characteristics
   The electrical characteristics in the Specifications may vary depending on ambient temperature, power supply voltage, circuit(s) externally applied, and/or other conditions. It is therefore requested to carefully check them including transient characteristics.
9. Not of a radiation-resistant design.
10. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.



11. Regarding input pin of the IC
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.
    Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



12. Ground Wiring Pattern
    When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
13. Operating ranges
    If it is within the operating ranges, certain circuit functions and operations are warranted in the working ambient temperature range. With respect to characteristic values, it is unable to warrant standard values of electric characteristics but there are no sudden variations in characteristic values within these ranges.
14. Thermal shutdown circuit
    This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the chip temperature reaches the threshold value listed below. When TSD is on, the device goes to high impedance mode. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature[℃] (typ.)
175	15

15. Heat sink (FIN)
    Since the heat sink (FIN) is connected with the Sub, short it to the GND.

Notes

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